Preliminary Reliability Evaluation of Copper-Interconnect Metallization Technology

Ashok K. Sharma
NASA Goddard Space Flight Center, Greenbelt, Maryland
Ashok.K.Sharma@gsfc.nasa.gov

Alexander Teverovsky
QSS Group Inc., Lanham, Maryland
Alexander.A.Teverovsky@gsfc.nasa.gov

Background

The advantages of using copper for interconnection in microcircuits are mostly due to its lower resistance compared to the aluminum metallization. Copper-based metallization has specific resistance of less than 2 μΩ-cm compared to more than 3 μΩ-cm for aluminum metallization. In combination with a reduced susceptibility to electromigration failures, this enables designing of highly scaled devices with significantly reduced time delays. These features are mostly beneficial for high-performance microprocessors and fast static RAMs (FSRAM).

In addition, copper interconnect process uses the dual damascene technology for deposition of copper, which can potentially reduce the manufacturing cost by eliminating some labor intensive steps of aluminum etching. This makes copper interconnect use quite attractive for semiconductor industry, and positions this technology as a standard interconnect process for the most high performance microcircuits in the future.

Major problems with copper metallization are due to some specific physical/electrochemical properties. Copper does not create a passive oxide film (as aluminum does), has poor adhesion and high rate of diffusion through silicon and dielectric layers (organic and inorganic). This introduces new failure mechanisms such as poisoning of the P-N junctions, charge instability and formation of resistive shorts caused by copper electrochemical migration.

The first on the market, copper-based FSRAM was manufactured by Motorola (the part is available since 1999). This part was used to gain experience with the copper-based interconnect design and technology, to analyze problems related to their evaluation and to obtain preliminary results of destructive physical analysis (DPA) of the parts.

Due to constraints caused by relocation of the GSFC Parts Analysis Lab, cross-sectional analysis of the part was performed by the Chipworks, Inc., Ottawa, ON, Canada [1].

Part Description

The XCM63R836RS3.3 is an 8M–bit synchronous, late write, fast static RAM designed to provide high performance in secondary cache and ATM switches, telecommunications, and other high speed memory applications. The part is organized as 256K words by 36 bits, and is fabricated in Motorola's high performance silicon gate CMOS technology (0.15 μm process). The technology employs copper interconnect metallization based on the damascene and dual- damascene processes.

The part features low cycle time of 3.3 ns, low power supply voltage of 3.9 V maximum for the core supply voltage and 2.5 V maximum for the output supply voltage. Operating temperature range of the part is specified as 0 °C to 70 °C, temperature under bias is –10 °C

to 85 °C, and storage temperature is –55 °C to 125 °C.

The part is designed as a Flipped Chip Ceramic Ball Grid Array (CBGA). Figure 1 shows external views of the part. It should be noted that no underfill compound was used in this design. The chip is mounted directly on a ceramic board using the flip-chip solder bump technology. Bottom side of the board has 119 solder bumps, which are organized in a 17×7 array with a 50 mil (1.27 mm) pitch.

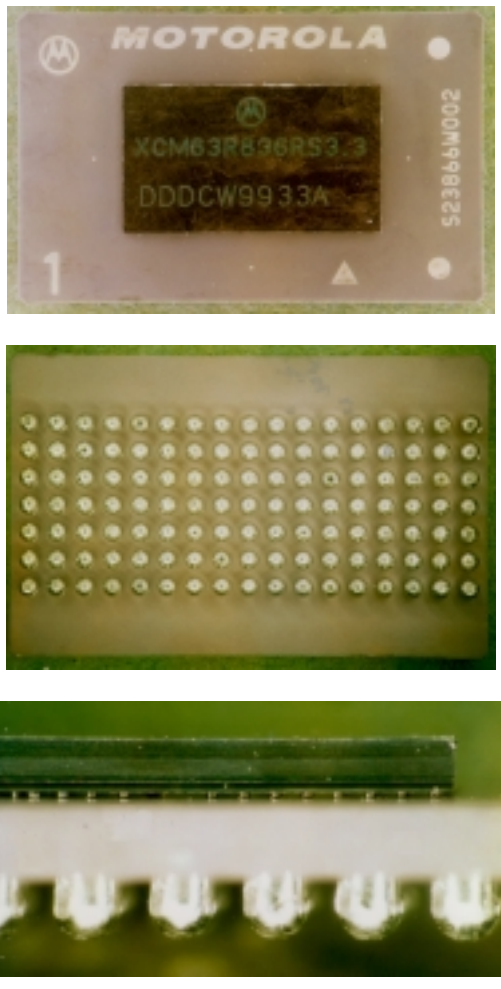


Figure 1 - External top, bottom, and side aspects of the part.

Processing And Reliability Challenges In Cu-Based Interconnect Metallizaton Microcircuits

Copper Damascene Process.

The damascene process, and its twin, the dual-damascene process, are considered to be the future technology of choice for laying metal lines and interconnects on chips [2]. The single greatest advantage is that the metal etch steps, which are notorious for process problems (corrosion, resist burn, time criticality with resist, etc) no longer exist, since all patterning is done with dielectric etching (currently, oxide etching). This enables previously unusable metals, in particular copper, to be reconsidered for interconnect metallization. Some of the key elements of copper damascene processes are described below.

Single Damascene. The fundamental difference of damascene relative to the standard processing is that the metal lines are not etched, but deposited in "grooves" within the dielectric layer, and then excess metal is removed by chemical-mechanical planarization (CMP) (Figure 2a).

Dual-Damascene. The differences of dual damascene relative to single damascene processing are that the plugs are filled at the same time as the metal lines. Several processing options exist for dual-damascene, and Figure 2b shows the currently preferred method, since the thickness of the metal lines can be accurately controlled.

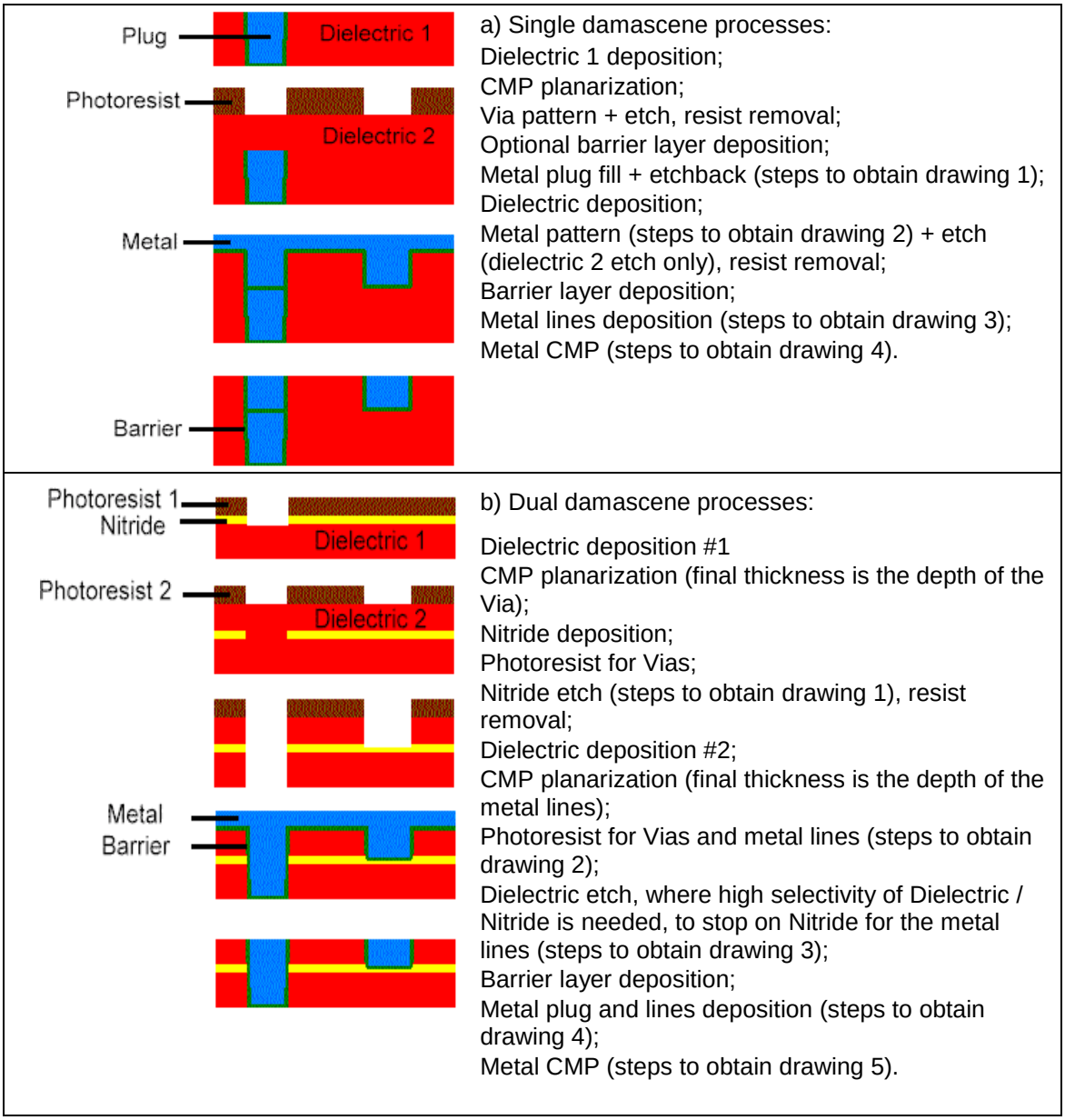


Figure 2 - Single (a) and dual (b) damascene processes.

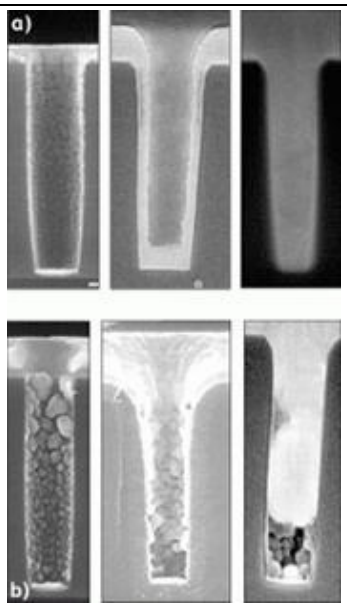
Process Challenges

Metal Deposition. The deposition of copper is made difficult since there is a need to fill holes and trenches, a requirement previously non-existent. Older physical vapor deposition (PVD) techniques were used for low aspect ratios (holes, which are not very deep or which. are wide), but they are not sufficient for the requirements of new designs.

Contemporary copper PVD seeding and subsequent fill by the electroplating technique have become the processes of choice to produce void-free fill of high-aspect-ratio (AR) damascene features [3]. Following the barrier layer, a thin continuous copper seed layer promotes adhesion and facilitates the subsequent growth of the bulk copper fill by electroplating.

To achieve high filling performance, the incoming feature profile, seed layer attributes, and key electroplating process and chemistry parameters must be optimized to encourage acceleration of deposition near the base of damascene features ("bottom-up" fill).

The success of copper plating to fill high AR features is built upon the achievement of successful nucleation followed by rapidly accelerated Cu deposition. Figure 3 shows examples of normal and defect-generating processes of copper deposition.



Cross-sectional via images showing (left to right):

a) smooth seed coverage only, metal profile following partial fill, complete fill by electroplating.

b) agglomerated seed coverage, metal profile following some electroplating, and resulting void at completion of electroplating.

Figure 3 - Normal (a) and defect-generating (b) via filling processes.

Copper Chemical Mechanical Planarization (CMP). Planarizing copper is no less challenging than depositing copper for the damascene interconnect structures. Development is complicated by new barrier materials and the material properties of copper itself [4]. Copper CMP is more complex, because of the need to remove the tantalum or tantalum nitride barrier layers without overpolishing any features. This is difficult because current copper deposition processes are not as uniform as the oxide deposition process. Finally, tolerances for erosion and dishing are much narrower for copper CMP process.

Copper has properties that add to the polish difficulties. Unlike tungsten, it is a soft metal and subject to scratching and embedded particles during polishing. Also, because copper is highly electrochemically active and does not form a natural protective oxide, it corrodes easily. Therefore, protecting the copper surface during polish, clean and subsequent processing are essential.

Barrier Layer. Copper can diffuse rapidly in silicon, silicon dioxide and low-k dielectrics, requiring that an impermeable barrier protect these dielectric layers. The barrier layer must prevent Cu diffusion, exhibit low film resistivity, have good adhesion to both dielectric and Cu, and be CMP compatible [5]. Also, the barrier layer must be conformal and continuous to fully encapsulate the Cu lines with as thin layer as possible. Due to the higher resistivity of the barrier material, its thickness should be minimized to allow for Cu to occupy the maximum cross-sectional area.

Much research had been performed to find the optimum, manufacturable barrier material and technology. Ta and

TaN_X were found to be best candidates for the microcircuits with the feature sizes below 0.25 µm. It was shown that the high temperature diffusion of copper decreases with the increase of nitrogen content.

Sealant Layer. Copper's oxidation characteristics introduce another problem. Cu oxidize relatively slow (the activation energy is about 1 eV) but forms a porous oxide with a weak adhesion. Unlike aluminum, in which initial oxidation forms a stable protective layer that prevents further oxidation, copper can oxidize indefinitely. In time, this oxidation can make copper interconnects unreliable. This poses additional problems during manufacturing and, in particular, wafer level testing. A silicon nitride film was found to provide adequate sealing for the copper metallization.

Copper Interconnect Inspection Challenges

Historically, more than 70% of the killer defects in microcircuits have been related to interconnects [6]. As such, with the introduction of new materials and fabrication techniques such as copper metallization and dual-damascene processes, defects associated with fill (voids, blocked etches, and particulates) issues will predominate. Thus, detecting hidden defects inherent in these processes becomes more difficult.

Due to special physical and chemical characteristics of copper, it will be beneficial only if it is properly processed, and insuring this may require regular process monitoring and qualification [7]. One of the most effective solutions to this problem is an employment of advanced automated e-beam system, which can detect process defects that cannot be captured by optical inspection or conventional e-beam techniques.

This advanced high-speed e-beam automated inspection systems (SEMSpec) combines a proprietary, high-brightness, thermal-field emission source, unique electron optics, and a high-speed image processor. The system inspects wafers using a low beam energy of 1.0 keV at scan speeds that are much faster than with the traditional SEMs.

The SEM image is digitized and sent to a computer, where defect detection algorithms determine the acceptability of the pattern. This e-beam technology offers high resolution and large depth of focus; it can find defects as small as 0.10 µm in size, even on densely packed, high-aspect-ratio, multilayer geometries.

Highly sensitive voltage-contrast imaging provides additional defect detection capability. Voltages induced on the surface of the circuit elements by the high beam current generate the voltage contrast. A bright electron source, high beam current, and a novel, energy-filtering secondary electron detection system, produces a high sensitivity for voltage-contrast imaging and detection at the wafer level. This identifies defects based on differences between properly and improperly formed structures and allows detection of defects at both the surface and deeper layers. Similar contrasts are difficult to observe in conventional e-beam approaches.

Cu-Interconnect Metallization Reliability Issues

Implementation of copper metallization is potentially beneficial for reliability of the microcircuits. The higher thermal conductivity of copper compared to the aluminum allows the metallization to conduct more heat away from the silicon die. This, together with the lower resistivity of copper, and consequently, lower heat dissipation in the metallization, would tend to reduce die temperature during operation, and thus improve performance and reliability of the part. Some of the key reliability issues are listed below.

Electromigration. Copper with its potentially higher electromigration

threshold as compared to aluminum is considered to be one of the most promising advantages for use of copper metallization for highly scaled microcircuits. However, some experiments indicate erratic behavior of thin copper lines under high current conditions [8]. Literature data shows a variance of the median time-to-failure (MTF) during electromigration tests from 6 hrs to 200,000 hrs for test conditions of 100 °C and 5×10^5 A/cm^2. This range is wider than the one observed for the conventional Al/Cu systems (85 hrs to 12,500 hrs).

This is mostly explained by the surface-dominated electromigration in the thin copper conductors. The metal-oxide interface, which is largely eliminated as a pathway for mass transport in Al is quite active in Cu. Lot-to-lot variations, even an issue with aluminum metallization, may be even worse for copper metallization.

The grain size to line width dependence is less important for the copper metallization than for the aluminum. This is most likely due to the specific of Cu lines structure, which are never perfect "bamboo" structures, but are generally bamboo-like, single-crystal across a given line.

Test data has shown, CVD-fill Cu lines exhibiting near-bamboo structure in sub-0.5-µm lines, moving to more mixed structures as linewidths increased, until becoming fully multicrystalline at 2 µm. However, the electromigration results were very close, which means that grain-boundaries cannot be the diffusion path for electromigration atomic flux [9]. The similarity between single- and multicrystalline line electromigration results supports the conclusion that the diffusion path is along the Cu barrier layer. If true, this suggests that the quality of the interface between the barrier and the copper seed layer is the single most important variable in the lifetime of Cu lines.

Electrochemical Migration. Application of copper metallization may introduce a new failure mechanism into the systems, which has never occurred with aluminum metallization, and that is the electrochemical migration, which can result in short circuit formation between the adjacent metallization stripes under DC bias [10].

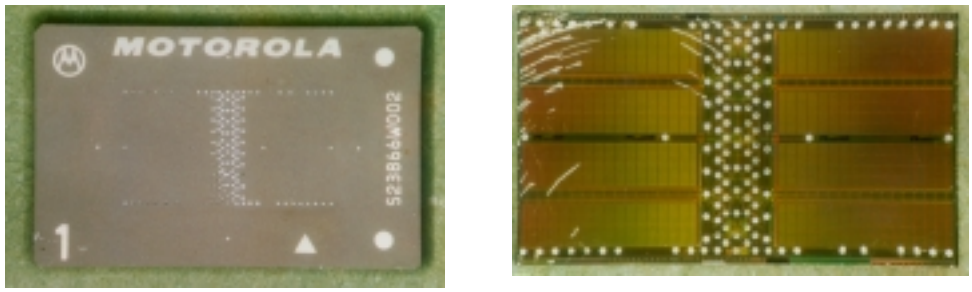
When a continuous moisture film or path occurs between two biased conductors, copper can be anodically dissolved from the positively biased line and redeposited in a dendritic form at the cathodic site. Similar failures may occur if sealing and passivation layers have pinholes and defects, which enable moisture penetration and condensation in the spacing between the copper interconnection lines.

Destructive Physical Analysis (Dpa) Of Cu-Interconnect 8m SRAMs

Optical Examination of the Die

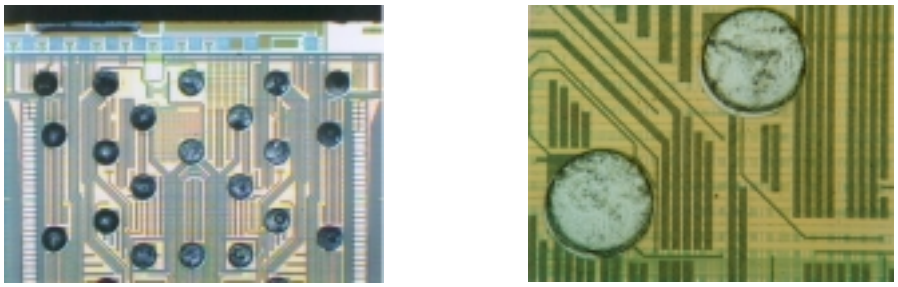
The die was removed from the ceramic board by heating up the assembly to approximately 250 °C. Figure 4 shows the ceramic substrate and the die after separation. The die had a size 12.1 mm X 7 mm and was covered with a relatively thick (approximately 4 µm) layer of polyimide film, which was removed by plasma etching for several hours. Figures from 5 to 7 show close-up views of the die surface and top level copper metallization. No patterning defects or any abnormalities on the die surface and/or the top-level metallization were observed.

Cross-Sectional Examination of the Die [The Chipworks, Inc. [1]]



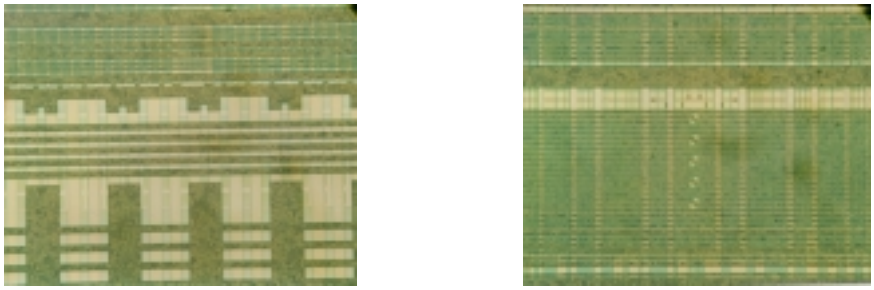
a) 4X b) 8X

Figure 4 - Ceramic substrate (a) and die (b) after the part deprocessing. The solder “threads” on the die surface (left top corner) were formed during desoldering. These "threads were located on the polyimide film and did not cause any damage to the die.



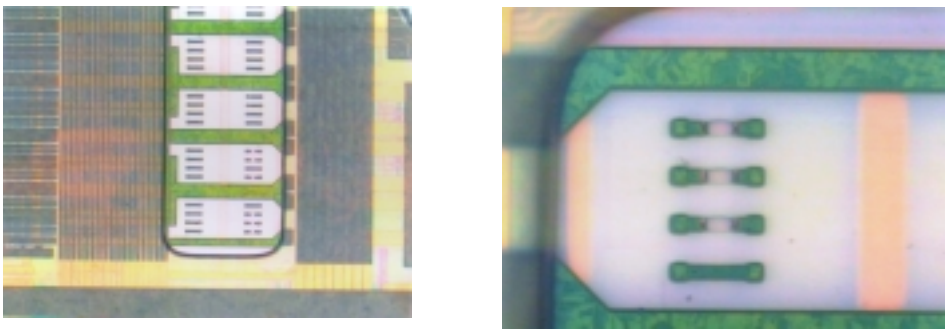
a) 50X b) 200X

Figure 5 - Close-up of the solder balls on the die.



a) 500X b) 500X

Figure 6 - Aspects of the top level copper metallization.



a) 200X b) 1000X

Figure 7 - Close-up of the fuses on the die surface.

Technique

One sample was cross-sectioned after decapsulation to evaluate dielectric and metallization properties. For objectivity, quality was assessed using MIL STD 883E, Class B criteria where appropriate, even though these devices were not procured to this specification. The dimensions used in this report are best estimates and have been obtained from the full library of images taken of this part. They are not necessarily measured from the images reproduced in this report.

Transmission Electron Microscope (TEM) analysis was performed to observe the microstructure of the copper and the barrier metal layer. Materials were identified using EDX (Energy Despersive X-ray) and EELS (Electron Energy Loss Spectrum). Secondary Ion Mass Spectrometry (SIMS) analysis was used to determine the overall concentration of different materials in the layers above the silicon substrate. Concentration traces are shown for the materials expected to be found in the device under analysis.

Die Processing Overview

The device structure utilizes four layers of copper metallization, one layer of tungsten local interconnect with tungsten plug contacts to the source/drains and gates. Shallow trench isolation is used throughout. A polysilicon layer forms the word lines and transistor gates and the minimum polysilicon wordline width is measured to be 0.15µm.

Copper Interconnect. The lowest copper layer is formed by the damascene technique 1 directly on to tungsten plug contacts. The successive copper layers are formed by the dual-damascene technique in which the contact plugs are created in the same deposition as the tracks. The anti-diffusion seal for the copper is tantalum. (No nitrogen was found in the tantalum). The lower three levels of copper tracks are sealed on the top surface by nitride. The uppermost copper layer is sealed with tantalum. Track thickness range from 0.38µm to 1.05µm and plugs range from 0.41µm to 0.76µm deep. The tantalum cap on the top metal layer is also used for fuse metallization.

Dielectric Layers. The silicon substrate and active regions are sealed with silicon nitride and several conformal layers of BPSG (Boron Phosphorus Silicon Glass), which are planarized by using CMP. Subsequent dielectric layers consist of a deposited silicon oxide layer with no boron or phosphorus doping. A silicon nitride (or oxynitride) sealant layer for the copper also acts as a diffusion barrier between the dielectric layers, and possibly an antireflection coating, while providing an indication of when to stop the CMP. The dielectric layers range from 0.24 µm to 0.84 µm in thickness.

A SIMS analysis of the dielectric layers was performed indicating that each layer with the exception of ILD1, was silicon dioxide. The ILD1 layer was BPSG composition. It is interesting to note that there is residual copper and aluminum coincident with the nitride sealant layers – probably due to absorbed copper and aluminum from an alumina-based CMP slurry.

0.18 µm Transistors. The wordline polysilicon width was measured at the cell access transistor gate oxide level on the FESEM cross-sectional micrographs and found to be 0.15 µm. The gate oxide is approximately 7 nm thick (see Figure 17).

Shallow Trench Isolation. The shallow trench isolation is about 0.33 µm. in depth and appears to be have a thermal oxide liner, which is then filled with CVD oxide and planarized by CMP (see Figure 17).

The die substrate is P+ type with an overlying P doped epitaxial layer. The die minimum dimension was 0.15 micrometers.

Tables 1 through 6 summarize constructional analysis of the 8 Mb SRAM. Figures 8 to 19 provide details of the construction analysis, design features, and various SEM/TEM cross-sectional view.

Table 1- Horizontal dimensions.

MinimumPadSize	120µm X l20um
MinimumPadWindow	65 µm. Diameter
MinimumPadSpace	202 µm.
MinimumMetal5width	1.94 µm.
MinimumMetal5space	1.56 µm.
MinimumMetal5pitch	3.50 µm.
MinimumMetal4width	1.7 µm.
MinimumMetal4space	1.7 µm.
MinimumMetal4pitch	3.4 µm.
MinimumMetal3width	0.35 µm.
MinimumMetal3space	0.52 µm.
MinimumMetal3pitch	0.88 µm.
MinimumMetal2width	0.43 µm.
MinimumMetal2space	0.35 µm.
MinimumMetal2pitch	0.78 µm.
MinimumMetallwidth	0.32 µm.
MinimumMetallspace	1.48 µm.
MinimumMetallpitch	1.8 µm.
Minimum Polywidth	0.15 µm
Minimum Polypitch	0.55 µm.
Minimum Polyspace	0.37 µm.
Cellsize	2.4um x l.8 µm.

Table 2 - Vertical Dimensions.

Die Thickness	0.70 mm.
Die coat	Polyimide 3.5 µm.
Passivation	Oxynitride 0.45 µm.
Metal5	1.05 µm (0.15um Ta + 0.8 µm Cu+0.10 µm Ta)
Interlayer dielectric (ILD)8	0.84 µm CVD oxide.
Sealant Layer (over copper metallization) on all dielectric layers above ILD2.	0.06 µm silicon nitride.
Metal4	0.5 µm (0.42 µm Cu+0.08 µm Ta)
ILDs7 and 6	0.28 µm CVD oxide+0.84 µm CVD oxide
Metal3	0.40 µm (0.32 µm Cu+0.08 µm Ta)
ILDs5 and 4	0.24 µm CVD oxide+0.84 µm CVD oxide.
Metal2	0.38 µm (0.3 µm Cu+0.08 µm Ta)
ILDs3 and 2	0.24 µm CVD oxide+0.4 µm CVD oxide.
Metal1	0.4 µm.
ILD1	0.57 µm BPSG+0.08 µm nitride
Plugs	0.76 µm.
Poly	0.15 µm.
Shallow Trench isolation	0.33 µm.

Table 3 - Dielectric Layers.

	Comments
Surface Oxide Defects	None observed.
Glassivation	0.45 μm oxynitride
Inner Layer Dielectric 8	0.84 μm oxide.
Sealant Layer (over copper metallizabon) on all dielectric layers above ILD2	0.06 μm silicon nitride.
Inner Layer Dielectric7	0.28 μm oxide.
Inner Layer Dielectric6	0.84 μm oxide
Inner Layer Dielectric5	0.24 μm oxide
Inner Layer Dielectric4	0.84 μm oxide
Inner Layer Dielectric3	0.24 μm oxide
Inner Layer Dielectric2	0.40 μm oxide
Inner Layer Dielectricl	0.60 μm BPSG (deposited in three layers) over 0.8 μm nitride layer.
Shallow Trench isolation	0.33 μm
Gate Oxide	≈7 nm.

Table 4 - Metallization.

	Plugs	Layer1
Type and Levels	Tungsten	CVD tungsten.
Minimum Dimension	0.30 μm	0.32 μm.
Minimum Spacing	0.22 μm	1.48 μm.
Minimum Pkch	0.52 μm	1.8 μm.
Thickness	0.76 μm	0.40 μm.
Quality	Good.	Good.
Voids	None observed	None observed.
Step Coverage	N/A	N/A

	Layer2	**Layer3**
Type and Levels	Dual-Damascene Copper Ta-Barrier Layer 0.08 um	Dual-Damascene Copper Ta-Barrier Layer 0.08 um
Minimum Dimension	0.43 μm	0.35 μm
Minimum Spacing	0.35 μm	0.53 μm
Minimum Pitch	0.78 pm	0.88 pm
Thickness	0.38 μm	0.40 μm
Quality	Good.	Good.
Voids	None observed.	None observed.
Step Coverage	N/A	N/A

Table 4 - Continued.

	Layer4	**Layer5**
Type and Levels	Dual-Damascene Copper Ta-Barrier layer 0.08 μm	Ta Capping Layer 0. 15 μm Dual-Damascene Copper Ta-Barrier layer 0.1 μm
Minimum Dimension	1.7 μm	1.94 μm
Minimum Spacing	1.7 μm	1.56 μm
Minimum Pitch	3.4 μm	3.50 μm
Thickness	0.50 μm	1.05 μm
Quality	Good.	Good.
Voids	None observed.	None observed.
Step Coverage	N/A	N/A

Table 5 - Polysilicon

	Comments
Type and Levels	Polysilicon
Siliciding Metal and Thickness	None observed.
Minimum Dimension	0.15 μm
Minimum Pitch	0.55 μm
Minimum Spacing	0.37 μm
Thickness	0.15 μm
Quality	Good.
Voids	None observed.

Table 6. Memory Cell.

	Comments
Cell Type	SRAM-6T
Cell Description	Load CMOS transistor
Storage Transistor Size(W/L)	0.33 μm/0.18 μm
Access Transistor Size(W/L)	0.33 μm/0.18 μm
Load Transistor Size(W/L)	0.33 μm/0.18 μm
Wordline Width/Pitch	0.18 μm/0.55 μm
Bitline Width/Pitch	0.43 μm/0.77 μm

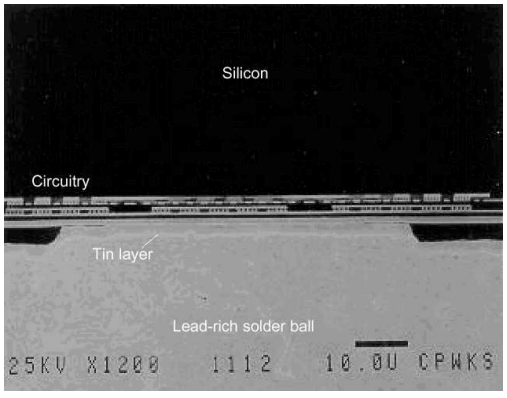


Figure 8.

SEM 1200X.

Cross-section through solder ball contact to pad metal.

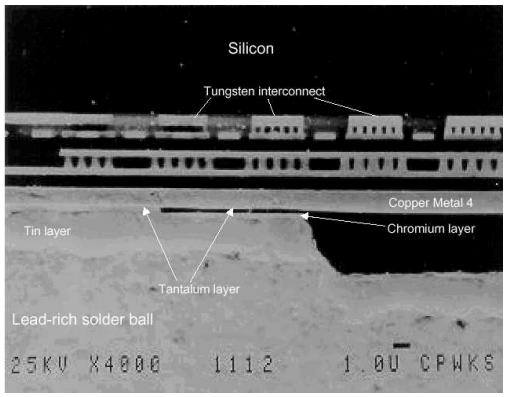


Figure 9.

SEM 4000X.

Cross-section through solder ball and pad metallization.

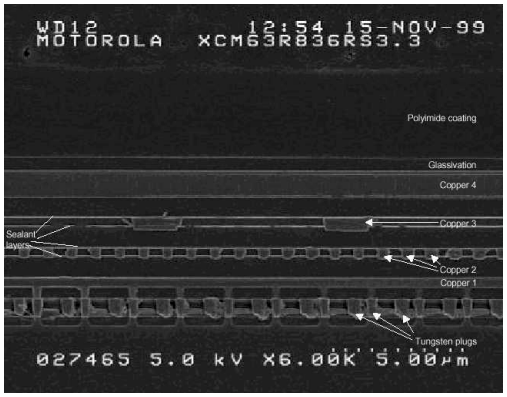


Figure 10.

SEM 6000X.

Cross-section through copper and tungsten metallization structure.

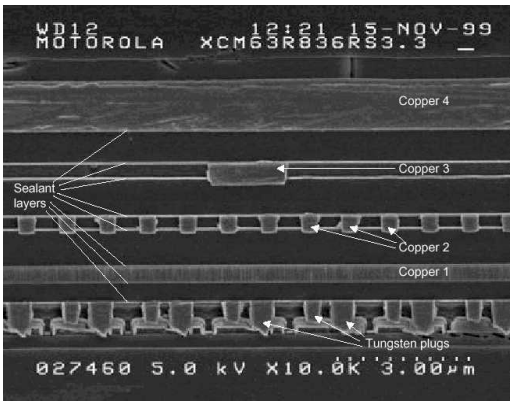


Figure 11.

SEM 10000X.

Cross-section through die metallization structure.

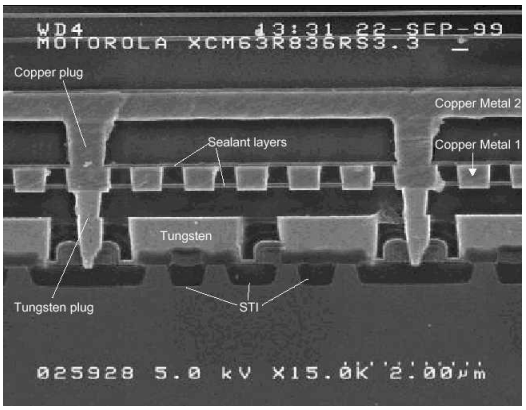
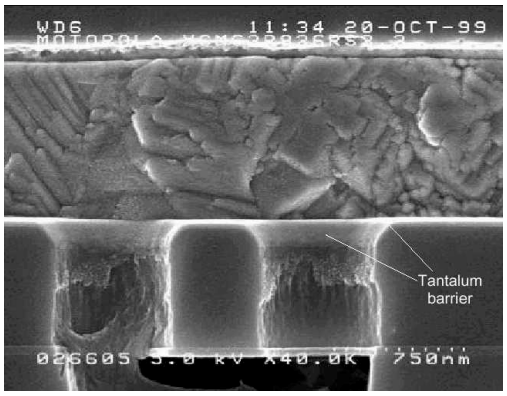
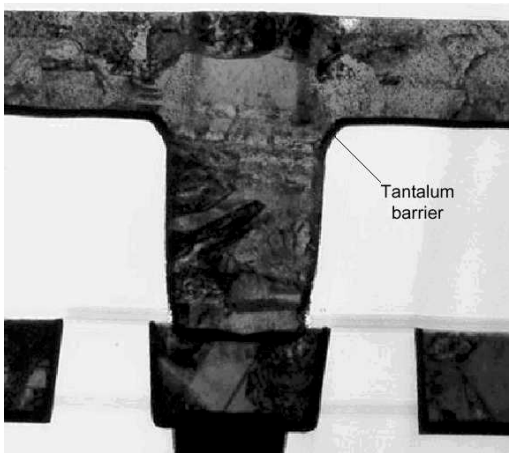
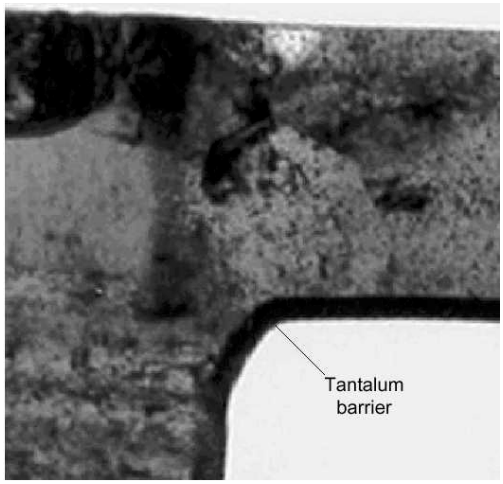
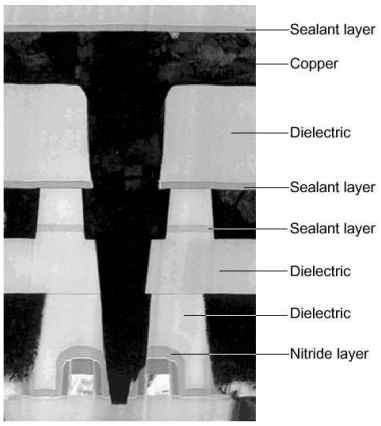
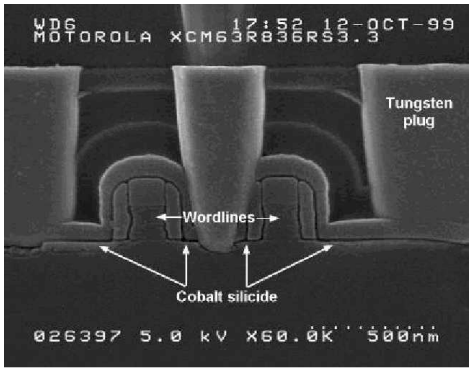
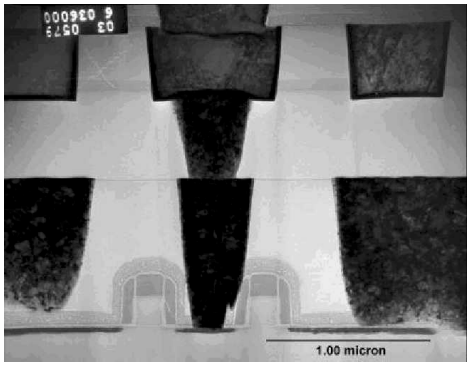
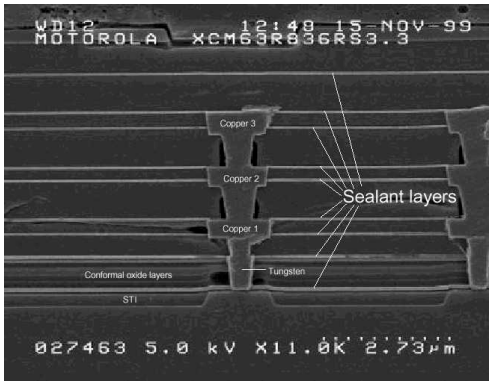


Figure 12.

15000X.

Cross-section through lower metal and dielectric layers.

	Figure 13. SEM 40000X. Cross-section through metal track high-lighting copper grain structure and tantalum barrier metal.
	Figure 14. TEM ~40000X. TEM image of cross-section showing copper grain structure and tantalum liner.
	Figure 15. TEM ~50000X. Closer view of tantalum barrier layer.

	Figure 16. TEM ~30000X. TEM image showing dielectric layers and sealant layers. Copper Sealant layer
	Figure 17. SEM 60000X. Cross-section through transistors and contacts.
	Figure 18. TEM ~39,800X. Cross-section through transistors and contacts.
	Figure 19. SEM 11000X. Cross-section of edge seal structure. (Dielectric fault is etching artifact).

Conclusions

Analysis of possible failure mechanisms specific to copper-based metallization shows that the presence of pores or defects in the sealant and/or barrier layers and voids in the copper-filled vias might have much more dramatic effect on reliability of the microcircuits compared to conventional microcircuits with aluminum metallization. The quality of sealant and barrier layers as well as the copper vias should be one of the prime concerns during destructive physical analysis of the part and might require development of special techniques for their evaluation.

The Motorola XCM63R836RS3.3 SRAM employs CMOS technology with four copper metal layers, one tungsten local interconnect layer and a single polysilicon layer. The copper metal interconnect layers are formed using dual-damascene processing with a tantalum-based barrier layer on the bottom and sides of the metal and silicon nitride sealant layer on the top. The top surface seal is formed with silicon nitride on all tracks except for the top-level metal tracks, which uses a thicker tantalum layer. This thicker cap layer is also used to form fuses. The device has tungsten local interconnect with tungsten plugs connecting to the source/drains and gates. The single polysilicon layer is not silicided in the array area. Peripheral circuitry in the SRAM is salicided with cobalt.

The construction analysis performed did not reveal any defects or obvious reliability concerns. However, test structures specially designed for a given Cu-Interconnect process evaluation, are required for technology assessment and validation.

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